Modelling of High-Frequency Capacitance-Voltage Characteristics of MOS Structures

Olumide Innocent Olope

DOI: 10.22178/pos.108-18

LCC Subject Category: T1-995

Received 30.08.2024
Accepted 25.09.2024
Published online 30.09.2024

Corresponding Author:
olumideolope@gmail.com

Abstract. This research explores the parameters and characteristics of Metal-Oxide-Semiconductor (MOS) structures. By employing equation systems that describe the processes at the metal-oxide-semiconductor interface, the capacitance-voltage (C-V) characteristics for RF probing signals were modelled. The study examined the dependence of volume charge density and specific capacitance on surface potential and gate-substrate voltage for p-type and n-type structures.

The calibration technology of the measurement setup was detailed, and enhancements to the calibration process were proposed. Sample preparation techniques for measurement were described, with the gate area measured at 1 mm². The technological stages of scribing and soldering microwires to the MOS structure were completed.

C-V characteristics for p-type and n-type MOS structure samples were obtained, and the dopant concentration and flat-band voltage were measured. A comparison between experimental and theoretical C-V characteristics revealed that a non-zero flat-band voltage causes both a shift and an extension of the C-V characteristic along the voltage axis. The total charge at the interface and within the dielectric was also quantified.

Keywords: MOS structure; Electronics; Nanoelectronics.

INTRODUCTION

Studying metal oxide semiconductor (MOS) structures is a cornerstone of semiconductor technology and the backbone of modern electronics. MOS structures are integral to the functioning of various electronic devices, including transistors, which are the building blocks of integrated circuits. Understanding these structures' electrical properties and behaviour is crucial for developing and optimising semiconductor devices.

High-frequency capacitance-voltage (C-V) measurements are a powerful analytical technique to probe MOS structures' electrical characteristics. These measurements provide detailed information about the interface quality, doping concentration, and charge distribution within the MOS device. Such insights are essential for improving the performance and reliability of MOS-based components.

This research investigates the volt-farad characteristics of silicon MOS structures at high frequencies, mainly focusing on the interplay between charge at the interface and charge within the dielectric. Understanding these characteristics is crucial as they reveal essential insights into the behaviour of MOS devices under varying electrical conditions.

The investigation begins with a theoretical exploration of the physical processes governing non-ideal metal-oxide-semiconductor contacts. This foundational understanding is complemented by computational simulations of the volt-capacitive characteristics of an ideal MOS structure using the Scilab mathematical package. By conducting these simulations, we aim to elucidate the behaviour of volt-capacitive characteristics, particularly the stretching effect observed along the voltage axis, attributed to full charge at the dielectric boundary.

Experimental analysis also plays a vital role in this study. We explore the differential capacitance dependence on bias voltage at a frequency of 1 MHz for both p-type and n-type MOS structures. This experimental approach is vital for validating our theoretical and simulation findings, providing a comprehensive understanding of the dielectric and semiconductor interface.

The calibration technology of the measurement setup is another critical aspect of this research. Accurate calibration is essential for obtaining reliable C-V measurements. This study describes the existing calibration technology and proposes enhancements to improve the accuracy and reliability of the measurements. These improvements are expected to reduce measurement errors and increase the precision of the C-V characteristics obtained.

Sample preparation is a vital step in the measurement process. The technology for preparing samples for C-V measurements is detailed in this research, including measuring the gate area, which was found to be 1 mm^2. The technological stages of scribing and soldering microwires to the MOS structure are also described. These steps ensure the samples are prepared correctly, and the measurements are reproducible.

The relevance of this research lies in its application to capacitance spectroscopy methods, which are essential for examining dielectric/semiconductor interfaces in advanced micro- and nanoelectronics. By employing these methods, we can accurately measure trap charge levels at the interface, a parameter that significantly influences the viability of materials for use as gate dielectrics or in memory elements. Moreover, the control of capacitance-voltage (C-V) characteristics is critical in the development of very large-scale integration (VLSI) circuits, where assessing the stability of gate dielectrics under thermal field tests can indicate shifts in flat zones of voltage, ensuring the reliability of semiconductor devices.

The novelty of this work lies in the comprehensive computer modelling of volt-capacitive characteristics conducted within the Scilab environment, alongside the investigation of unique behaviours in actual MOS structures. These behaviours, particularly stretching the characteristic graphs along the voltage axis, further our understanding of charge dynamics within dielectric boundaries. This study aims to contribute significantly to the existing body of knowledge, paving the way for improved applications and advancements in semiconductor technology.

In summary, this research aims to bridge the gap between theoretical predictions and experimental observations of MOS structures. By developing a comprehensive model for the high-frequency C-V characteristics and improving the calibration and sample preparation technologies, this study contributes to the optimisation of MOS device fabrication and performance. The findings are expected to pave the way for advancements in semiconductor technology, enhancing the performance and reliability of electronic devices.

Capacitance-voltage characteristics of MIS structures

The structure of the MIS structure and its energy diagram. Metal-insulator-semiconductor structures, or MIS structures for short, owe their widespread interest in studying their physical properties to the advent of planar technology and the development of a new class of semiconductor devices operating based on the field effect, such as charge-coupled devices., insulated gate field-effect transistors, reprogrammable floating gate memory elements, etc. MIS structures allow us to analyse the main processes occurring in such devices and are highly convenient objects of study. The design of an MIS structure follows from its name.

An MOS structure is a single-crystal semiconductor plate, called a substrate, covered with a dielectric on the planar side. The metal electrode applied to the dielectric is called a gate, and the dielectric is called a gate. A metal electrode, an ohmic contact, is applied to the reverse non-planar side of the semiconductor plate. Often, oxides are used as a dielectric in MOS structures; therefore, MOS structure is used instead of MOS. Thus, the MOS structure shown in Figure 1 consists of a gate, a gate dielectric, a semiconductor substrate, and an ohmic contact.

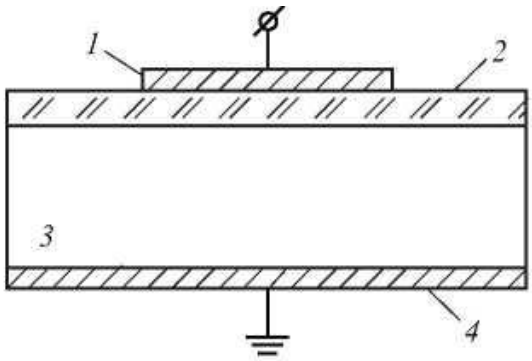

Figure 1 – MOS structure: 1 - gate, 2 - gate dielectric, 3 - semiconductor substrate, 4 - ohmic contact

Let us consider the energy band diagram of the MOS structure under equilibrium conditions. According to the rule for constructing band diagrams, it is necessary that in the system, in the absence of applied voltage: a) the vacuum level was continuous; b) the electron affinity of the

dielectric and semiconductor at each point was constant; c) the Fermi level was the same.

Figures 2b, 2c show the band diagrams of ideal MIS structures for different applied voltage polarities. VGto the shutter.

MIS structures close to the ideal are obtained using the "chlorine" technology of thermal growth of silicon dioxide on silicon, with aluminium used as the gate material for n-Si and P-Sigold.

MIS structures in which one of the above requirements is violated are called actual MIS structures, the properties of which are discussed below.

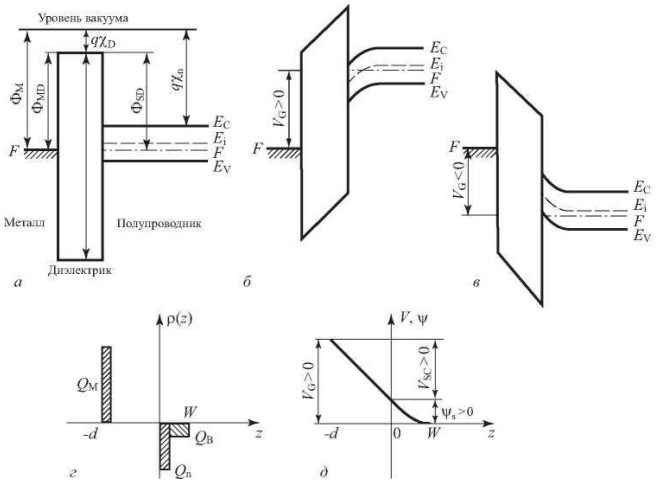

Figure 2 – Band diagram of an ideal MIS structure with a p-type semiconductor: a) V_G=0; b) V_G>0; c) V_G<0 charge distribution in the MIS structure with V_G>0; d) distribution of applied voltage V_G between dielectric and semiconductor

Electroneutrality equation. Let's take a closer look at the relationship between the gate voltage V_G MIS structures and surface potential ψ_G. All applied voltage$V_G$to the MIS structure is divided between the dielectric and the semiconductor, and it is evident that the voltage drop in the semiconductor is equal to the surface potential ψ_G. Thus,

$$V_G = V_{OX} + \psi_G \quad (1)$$

From (1) and the analysis of the band energy diagrams, it follows that the sign of the surface potential ψ_G, which we chose earlier a priori, actually corresponds to the sign of the gate voltage V_G. Indeed, a positive voltage on the gate of an ideal MIS structure causes a downward bending of the bands in n- and p-type semiconductors, corresponding to positive surface potential values. A negative voltage V_G causes an upward bending of the bands at the surface of the semiconductor, which corresponds to a negative value of the surface potential ψ_S.

From the condition of electrical neutrality, it follows that the charge on the metal electrode Q_M must be equal to the total charge in the SPRQ_{SC}, the charge of surface states at the semiconductor-insulator interface Q_{SS} and the built-in charge in the dielectric near the interface Q_{OX}. Then,

$$-Q_M = Q_{SC} + Q_{SS} + Q_{OS} \quad (2)$$

According to the definition of the geometric capacitance of a dielectric C_{OX}:

$$C_{OX}=Q_M/V_{OX} \quad (3)$$

from here

$$V_{OX} = \frac{Q_M}{C_{OX}} = -\frac{Q_{SC}}{C_{OX}} - \frac{Q_{SS}}{C_{OX}} - \frac{Q_{OS}}{C_{OX}} \quad (4)$$

Considering that there is a difference in thermodynamic work functions between a metal and a semiconductor $\Delta\varphi_{ms}$, we get:

$$V_G = \Delta\varphi_{ms} + \psi_s - \frac{Q_{SC}}{C_{OX}} - \frac{Q_{SS}}{C_{OX}} - \frac{Q_{OS}}{C_{OX}} \quad (5)$$

From (5), it follows that if V_G>0, that, i.e. voltage drops across the dielectric V_{ox}>0. The sign relation will be similar. As we have shown earlier, that

$$Q_{ss} = -qN_{ss}(\psi_s - \varphi_0) \quad (6)$$

substituting (6) into (5), we get:

$$V_G = \Delta\varphi_{ms} - \frac{Q_{SC}}{C_{OX}} - \frac{qN_{ss}}{C_{OX}}\varphi_0 + \\ +\psi_s - \frac{Q_{OS}}{C_{Os}} + \frac{qN_{ss}}{C_{Os}}\psi_s \quad (7)$$

Let us introduce a new notation — the flat band voltage VFB (Flat Band). The flat band voltage VFB is the voltage on the gate of an actual MIS structure, corresponding to the value of the surface potential in the semiconductor equal to zero:

$$V_{FB} = V_G(\psi_s = \varphi_0) \quad (8)$$

Taking into account definition (8), it follows from (7):

$$V_{FB} = \Delta\varphi_{ms} - \frac{Q_{ox}}{C_{OX}} + \frac{qN_{ss}}{C_{OX}}\varphi_0 \quad (9)$$

Thus, the relationship between the gate voltage VG and the surface potential, taking into account (9), is given in the form:

$$V_G = V_{FB} + \psi_s + \frac{qN_{ss}}{C_{Ox}}\psi_s - \frac{Q_{SC}}{C_{os}} \quad (10)$$

Let us conduct a more detailed analysis (10) for different regions of surface potential change.

Enrichment (Vs< 0)

The expression for the charge in the SCRQsc is described by the relation (19). Substituting (19) into (1), we obtain:

$$V_G - V_{FB} = \psi_s\left(1 + \frac{qN_{ss}}{C_{Ox}}\right) - \frac{2\varepsilon_s\varepsilon_0 kT}{qL_D C_{os}} e^{\frac{B\psi_2}{2}} \quad (11)$$

For large values $\psi_s(/B\psi_2/>1)$, when Qsc>>Qss, from relation (11), it follows:

$$V_G - V_{FB} = -\frac{2\varepsilon_s\varepsilon_0 kT}{qL_D C_{os}} e^{-\frac{B\psi_2}{2}} \quad (12)$$

From here

$$\psi_s = \frac{-2kT}{q}\ln\left[(V_G - V_{FB})\frac{qL_D C_{os}}{\varepsilon_s\varepsilon_0 kT}\right]$$

$$Q_{sc} = Q_p \approx -C_{0x}(V_G - V_{FB}) \quad (13)$$

From (12) and (13) it follows that when the surface is enriched with holes as the leading carriers, the surface potential depends on the gate voltage V_G logarithmically, and the charge Q_{sc}in the OPZ depends on the gate voltage V_G linearly.

Depletion and weak inversion ($0 < \psi_s$<**2**φ_0*)*

Charge in OPZQ_{sc} in this case, it is mainly due to ionised acceptors Q_B and is expressed by the relation (20).

Let's expand the expression for Q_B in a row close by ψ_s=φ_0:

$$Q_B = Q_B(\psi_s=\varphi_0) + \frac{\partial Q_B}{\partial \Psi_s}((\psi_s-\varphi_0) =$$

$$= Q_B^* + C_B^*((\psi_s-\varphi_0)$$

where Q_B^*, C_B^*— the magnitude of the charge and capacity of ionised acceptors in the SCR at

Substituting the expression for into (10) and taking into account the expression for C_B^*, we get:

$$V_G - V_{FB} = N\psi_s \quad (14)$$

$$\text{where } N = 1 + \frac{qN_{ss}}{C_{Os}} + \frac{C_B^*}{C_{Os}} \quad (15)$$

From (14), it follows that in the region of depletion and weak inversion, the surface potential ψ_s depends on voltage V_G linearly, and the tangent of the angle of inclination

$$lg\ \alpha = \frac{dV_G}{d\psi_s} = n$$

is determined by the density of surface states Nss, thickness of the gate dielectricdox, and the doping level of the semiconductor substrate NA.

Strong inversion ψ_s>$2\varphi_0$

Charge in OPZQ scnegative, consists of the charge of ionised acceptors QBand electrons Qnin the inversion layer. For Qn, we have:

$$V_G = \Delta\varphi_{ms} - \frac{Q_{ox}}{C_{OX}} - \frac{qN_{ss}}{C_{OX}}\varphi_0 - \frac{Q_B}{C_{Ox}} +$$

$$+2\varphi_0 - \Delta\psi_s + \frac{qN_{ss}}{C_{Ox}}\Delta\psi_s + \frac{\varepsilon_s\varepsilon_0 kT}{qL_D C_{os}} e^{\frac{B\psi_2}{2}} \quad (16)$$

where is the value $\Delta\psi_s = \psi_s - 2\varphi_0$.

Let's introduce the threshold voltage VTas gate voltage VG, when under equilibrium conditions, the surface potential $\psi_s$equal to the threshold value $2\varphi_0$.

$$V_T = V_{G(\psi_s=2\varphi_0)} \quad (17)$$

From (16) and (17) it follows that

$$V_T = \Delta\varphi_{ms} + 2\varphi_0 - \frac{Q_{ox}}{C_{OX}} + \frac{qN_{ss}}{C_{OX}}2\varphi_0 - \frac{Q_B}{C_{Ox}} \quad (18)$$

or taking into account the definition VFB.

Experimental method for determining the average doping concentration based on the maximum and minimum high-frequency capacitance

Let us consider the processes in the near-surface region of a semiconductor in the case where an electric field is applied perpendicular to the surface using a metal electrode.

The MIS structure can be likened to a capacitor, one plate of which is a metal (upper electrode) and the other (near-surface region) is the surface of a semiconductor. Switching on a field of different polarity causes either enrichment of the near-surface layer of the semiconductor with the leading carriers (on the metal, "+" semiconductor type) or depletion (on the metal, "", semiconductor type). A change in the concentration of free charge carriers under the action of an electric field should lead to a change in conductivity along the surface of the sample. This phenomenon is called the field effect and is the basis for the operation of MIS transistors.pn

An essential property of the MIS structure is the dependence of its capacity on the applied voltage. This dependence is because the thickness of the surface layer, depleted or enriched in charge carriers, changes with a change in the applied voltage. The operation of the MIS varactor is based on this effect.

Figure 3 shows the band diagram of an ideal MIS structure with a band bend corresponding to the depletion layer for ap -type semiconductor.

A positive voltage is applied to the metal.

ψ_S - surface potential, in this case; $\psi_S > 0$

ψ_B - potential difference between the Fermi level and the Fermi level of the intrinsic semiconductor $E_F E_i$.

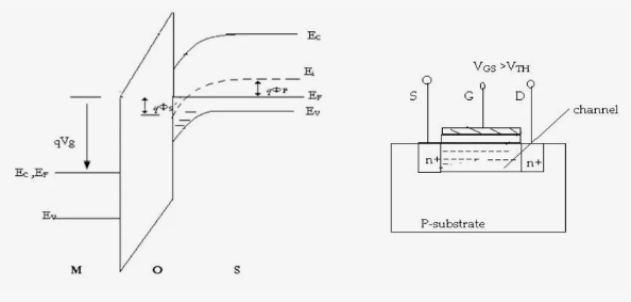

Figure 3 – Band diagram of an ideal MIS structure with band bending corresponding to the depletion layer for ap -type semiconductor

An ideal MIS structure satisfies the following conditions:

1. At zero bias, the difference between the work functions of the metal and the semiconductor is zero;

2. When a bias is applied, the charge generated in the structure consists of the charge generated in the semiconductor and the charge of the opposite sign on the metal separated from the semiconductor by the insulator. In other words, there are no surface states at the semiconductor-insulator interface, which are usually charged.Q_S

3. There is no movement of charges through the dielectric under constant bias conditions, i.e. the dielectric is ideal, and its resistance is infinite.

The total capacitance of the MOS structure consists of the series-connected capacitance of the dielectric and the surface capacitance of the semiconductor $C_д C_S$.

$$\frac{1}{C} = \frac{1}{C_д} + \frac{1}{C_S} \text{ or } C = \frac{C_д C_S}{C_S + C_д}$$

The capacity of the entire MIS structure can be expressed as follows:

$$\frac{1}{C_{МДП}} = \frac{1}{C_{OK}} + \frac{1}{C_{SC} + C_{SS}}$$

If the difference between the work functions of a metal and a semiconductor is not equal to zero, then the current-voltage characteristic shifts relative to the theoretical ("ideal") characteristic along the voltage axis by an amount equivalent to the difference in the work functions.

At $\Delta\phi_{МП} < 0$the shift occurs in the direction of positive bias on the metal while in the direction

of negative bias. The presence of surface states and charge in the oxide also causes a shift in the capacitive volt-ampere characteristics in one direction or another from the theoretical ones, depending on the sign of the surface charge $\Delta\phi_{\text{МП}} > 0$.

The noted property of the capacitive-voltage characteristics determines the density of surface states. To ensure flat band conditions, it is necessary to apply an additional bias that compensates for the charge causing the band bending. The magnitude of this bias (flatlands) allows us to estimate the total charge at the semiconductor-dielectric interface $\Delta V_{FB} Q_S$.

$$\Delta V_{FB} = \frac{Q_S}{C_{OK}} + \Delta\phi_{\text{МП}}$$

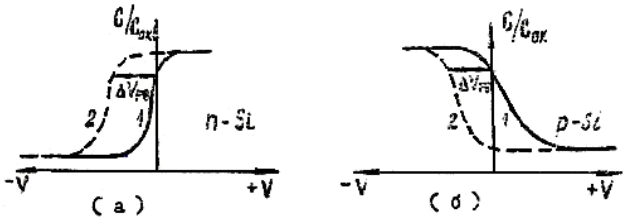

Figure 4 – Volt-farad curves a – silicon-type, b – silicon-type np

The shift of the experimental curve of the MOS structure (2) relative to the theoretical one (1) is caused by surface states $C - V$.

Neglecting the magnitude of the contact potential difference, one can use the shift in the experimental$C - V$characteristics from theoretical () to determine the magnitude of the charge and, accordingly, the density of surface states using the formula $\Delta V_{FB} Q_{SS} N_{SS}$.

$$N_{SS} = \frac{Q_{SS}}{q} = \frac{C_{OK}\Delta V}{q}$$

The capacitance-voltage characteristic can be used to determine the impurity concentration. When the surface layer is depleted of charge carriers, the charge density Q_{SS} cannot increase indefinitely and is limited by the charge density of the ionised impurity atoms. Therefore, as the applied voltage increases, when the conditions for the formation of an inversion layer are not met, the maximum width of the space charge region will be uniquely determined by the concentration of donors (acceptors) at a depth equal to the boundary of the depleted layer. We present an expression obtained from solving the Poisson equation $qNdd$.

$$d = \sqrt{\frac{\varepsilon kT}{4\pi q^2 N}}$$

where ε-dielectric constant of a semiconductor; k - Boltzmann constant; T - temperature; q - electron charge; N - impurity concentration equal to the concentration of free carriers.

As is known, the capacity, in this case, has a minimum value. Knowing and calculating from the value one can determine and then $C_{min} C_{OK} C_S dN$.

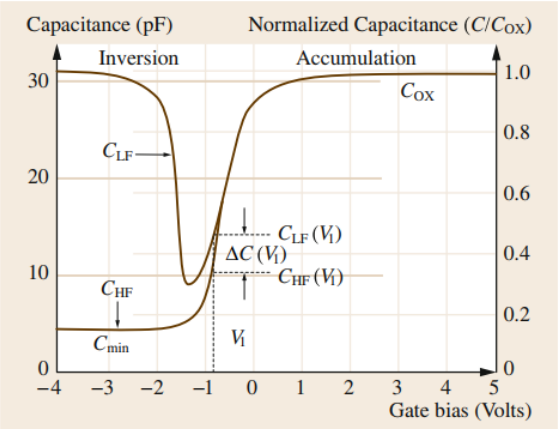

Figure 5 – Typical volt-capacitance characteristic of n-type MOS structure at HF and LF

The method based on determining the maximum and minimum high-frequency (HF) capacitance uses the HF capacitance at substantial accumulation and strong inversion to determine the average doping density. It should be noted that the capacitance of surface traps is insignificant at strong inversion and high frequencies. At solid inversion, the depletion width is maximum, so the HF capacitance per unit area is minimum (since minority carriers cannot have a response to a high-frequency signal). Since the inversion layer is skinny compared to the depletion layer, then $C_{OX} C_{HF,min} C_{IT} \approx 0 \omega_{max} C_{HF,min}$.

$$w_{\max} = \varepsilon_{\text{Si}} \left(\frac{1}{C_{\text{HF,min}}} - \frac{1}{C_{\text{OX}}} \right),$$

where is the permittivity of silicon and is the capacitance of the gate oxide per unit area.

Provided that the band bending is maximum, it is determined by $\varepsilon_{Si} C_{OX} \omega_{max}$

$$\psi_{\max} = 2\phi_B + \frac{kT}{q} \ln\left(2\frac{q}{kT}\phi_B - 1\right) = 2\frac{kT}{q}\left\{\ln\left(\frac{n}{n_i}\right) + \frac{1}{2}\ln\left[2\ln\left(\frac{n}{n_i}\right) - 1\right]\right\} \quad (19)$$

where the shift of the Fermi level from the intrinsic Fermi level in the bulk of silicon in the MOS structure is at a doping concentration of n.

Here is the intrinsic carrier concentration in silicon due to thermal generation. For a uniformly doped sample, $\phi_B = (k_B T/q) \cdot ln(n/n_i)\phi_i = (E_c - E_v)/2\, qn_i$

$$w_{\max}^2 = \frac{2\varepsilon_{Si}\psi_{\max}}{qn} \quad (20)$$

From (19) and (20), the relationship between the doping concentration n and the measured capacitance can be reduced to the form

$$\frac{n}{\ln\left(\frac{n}{n_i}\right) + \frac{1}{2}\ln\left[2\ln\left(\frac{n}{n_i}\right) - 1\right]} = \frac{4kT}{q^2\varepsilon_{Si}} \frac{C_{OX}^2}{\left(\frac{C_{OX}}{C_{HF,min}} - 1\right)^2}. \quad (21)$$

Equation (21) is a transcendental equation for the average. In a single figure, the solutions of the equation can be plotted against the oxide thickness. This can be used to determine the average doping value *n* graphically. Equation (21) can be further simplified by neglecting the term and assuming that. In addition, an approximation (21) for the average doping concentration n in unity can be obtained for silicon MOS structures at room temperature and is given by

$$C_{HF,min}/C_{OX}\ 0.5 \cdot ln[2ln(n/n_i)]C_{OX} = C_{HF,min}\text{см}^{-3}$$

$$\log_{10}(n) = 30.38759 + 1.68278 \times \log_{10}(C_{DM} - 0.03177) \times [\log_{10}(C_{DM})]^2, \quad (22)$$

where the depletion capacitance (per area) is defined ascм$^2 C_{DM}$

$$C_{DM} = \frac{C_{HF,min} C_{OX}}{C_{OX} - C_{HF,min}} \quad (23)$$

Modelling of capacitance-voltage characteristics in Scilab

The simulation of the volume charge density ρ was carried out with the following constants and parameters: $q = 1{,}6 \cdot 10^{-19}$ Кл; $n_i = 1{,}45 \cdot 10^{10}\text{см}^{-3}$; $N_a = 1.0 \cdot 10^{16}\text{см}^{-3}$; $N_d = 1.0 \cdot 10^{16}\text{см}^{-3}$; $T = 300\ K$; $k = 1{,}38.10^{-23}$ Дж/К; $-1{,}2\text{В} < \varphi_s < 1{,}2\text{В}$.

According to the formulas:

$\varphi_t = kT/q$ - temperature potential;

$\varphi_f = \varphi_t \cdot ln(N_a/n_i)$ - the potential difference between the Fermi level and the Fermi level of an intrinsic p-type semiconductor;

$\varphi_f = -\varphi_t \cdot ln(N_d/n_i)$ - the same for n-type semiconductors;

$p_{p0} = n_i \cdot exp(\varphi_f/\varphi_t)$ - equilibrium concentration of holes in a p-type semiconductor (Hole concentration at thermal equilibrium)

$n_{p0} = n_i \cdot exp(-\varphi_f/\varphi_t)$ - equilibrium concentration of electrons in a p-type semiconductor (Electron concentration at thermal equilibrium);

$p_{n0} = n_i \cdot exp(\varphi_f/\varphi_t)$ – equilibrium concentration of holes in an n-type semiconductor (Hole concentration at thermal equilibrium);

$n_{n0} = n_i \cdot exp(-\varphi_f/\varphi_t)$ – equilibrium concentration of electrons in an n-type semiconductor (Electron concentration at thermal equilibrium);

$\rho_0 = q \cdot \left(n_{p0} - p_{p0} + p_{p0} \cdot exp(-\varphi_s/\varphi_t) - n_{p0} \cdot exp(\varphi_s/\varphi_t)\right)$ – volume charge density near the surface of the p-MOS structure;

$\rho_0 = q \cdot \left(n_{n0} - p_{n0} + p_{n0} \cdot exp(-\varphi_s/\varphi_t) - n_{n0} \cdot exp(\varphi_s/\varphi_t)\right)$ – volume charge density near the surface of the n-MOS structure.

The simulation results are shown below.

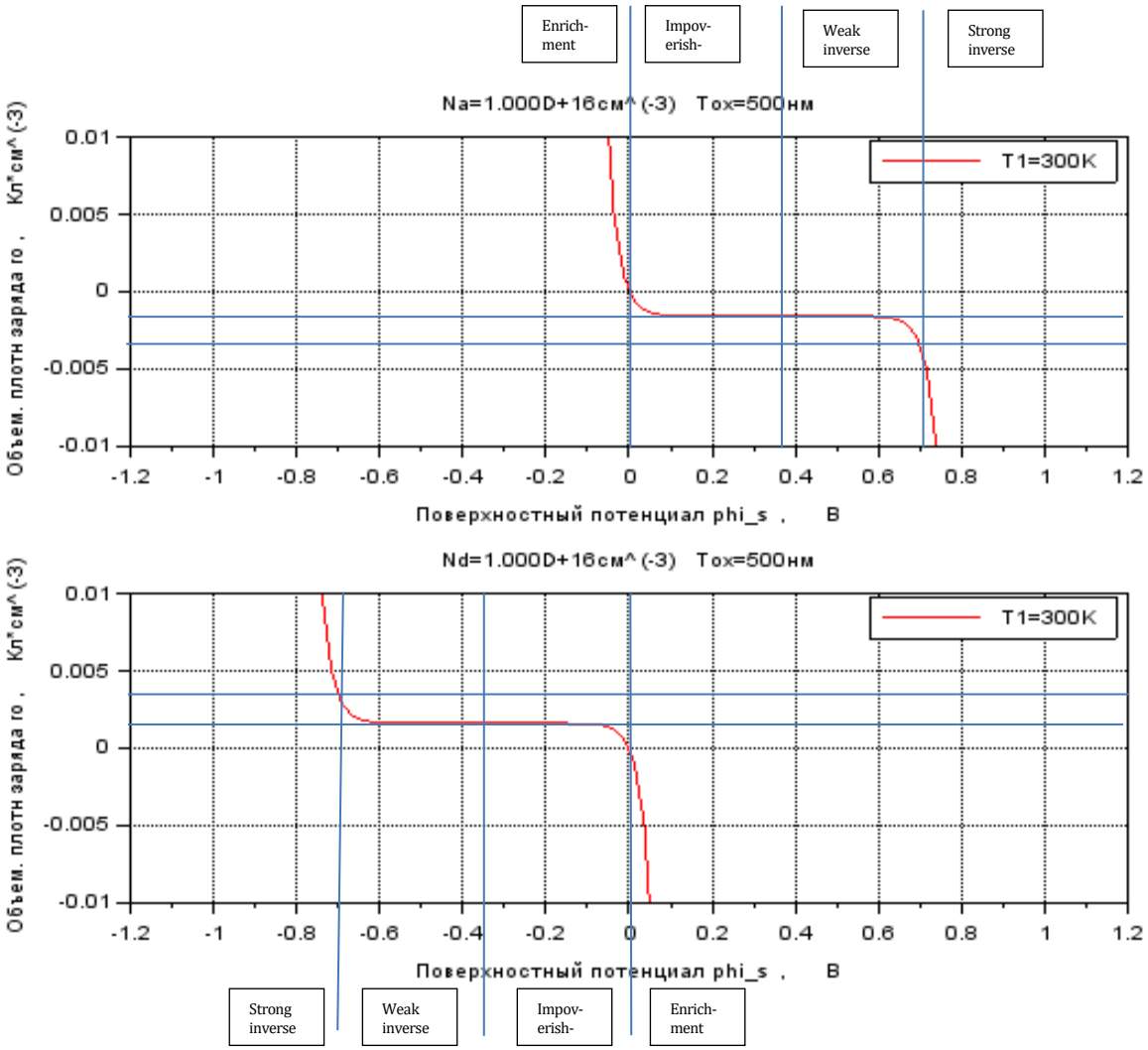

Figure 6 – Simulated dependence of the volume charge density in a semiconductor near the surface of an MOS structure on the surface potential for p-type (top) and n-type (bottom) $\rho_0\varphi_s$

For the p-type, as can be seen from the upper graph, the accumulation mode occurs for room temperature T=300K at φs<0V. When the curve sharply increases, at 0<φs<0.38V, the depletion mode occurs - to the left of the symmetry axis, at 0.38V<φs<0.7V, the weak inversion mode occurs - to the right of the symmetry axis, at φs>0.7V the robust inversion mode occurs when the curve sharply decreases.

For the n-type, as seen from the lower graph, the modes replace each other in reverse order.

Modelling the dependence of specific capacity C'_{eq}MOS structures from surface potential φ_s was carried out with the following values of constants and parameters: $\epsilon_o = 8{,}854 \cdot 10^{-14}$ Ф/см$^{-1}$; $\epsilon_{Si} = 11{,}7\epsilon_o$; $\epsilon_{OX} = 3{,}97\epsilon_0$; $T_{ox} = 500 \cdot 10^{-7}$ см; using the following relationships:

$A_{HF} = 1 - exp(-\varphi_s/\varphi_t) + exp(-2\varphi_f/\varphi_t) \cdot (0 \cdot exp(\varphi_s/\varphi_t) - 1)$ for p-type;

$B_{HF} = 2 \cdot \left(\varphi_t \cdot exp(-\varphi_s/\varphi_t) + \varphi_s - \varphi_t + exp(-2\varphi_f/\varphi_t) \cdot (0 \cdot \varphi_t \cdot exp(-\varphi_s/\varphi_t) + 0 \cdot \varphi_s - \varphi_t)\right)^{1/2}$ - for p-type;

$A_{HF} = -1 + exp(-\varphi_s/\varphi_t) + exp(2\varphi_f/\varphi_t) \cdot (0 \cdot exp(\varphi_s/\varphi_t) - 1)$ - for n-type;

$B_{HF} = 2 \cdot \left(\varphi_t \cdot exp(\varphi_s/\varphi_t) - \varphi_s - \varphi_t + exp(2\varphi_f/\varphi_t) \cdot (0 \cdot \varphi_t \cdot exp(-\varphi_s/\varphi_t) + 0 \cdot \varphi_s - \varphi_t)\right)^{1/2}$ - for n-type;

$C'_{sc} = (2 \cdot q \cdot \epsilon_{Si} \cdot N_a)^{1/2} \cdot A_{HF}/B_{HF}$, $If \varphi_s > 0$, $C'_{sc} = -(2 \cdot q \cdot \epsilon_{Si} \cdot N_a)^{1/2} \cdot A_{HF}/B_{HF}$, $If \varphi_s < 0$ - specific capacitance of the semiconductor; $C'_{ox} = \epsilon_{OX}/T_{ox}$ - specific capacity of oxide; $C'_{eq} = C'_{ox} \cdot C'_{sc}/(C'_{ox} + C'_{sc})$ - specific capacitance of the MOS structure.

The results of modelling the normalised specific capacity are shown in Figure 7, C'_{eq}/C'_{ox}.

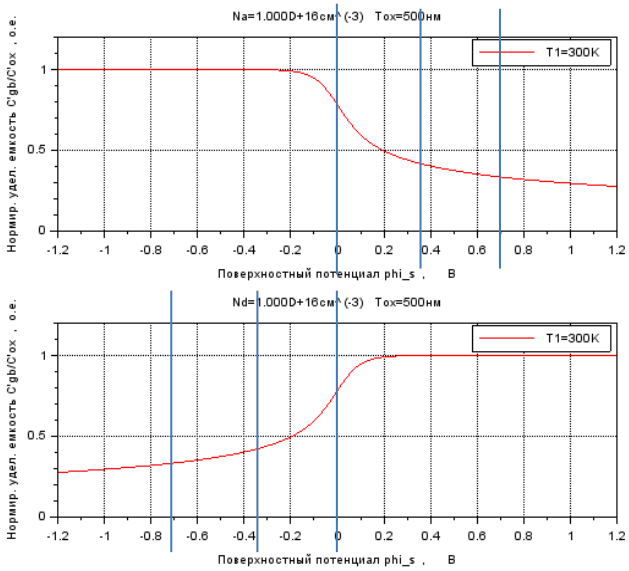

Figure 7 – Simulated dependence of the normalised specific capacitance of the MOS structure on the surface potentialC'_{eq}/C'_{ox} $\varphi_s$for p-type (top) and n-type (bottom)

Modelling the dependence of specific capacity C'_{eq}MOS structures from gate-substrate surface voltage were carried out using the following relationships:

$B = 2 \cdot \left(\varphi_t \cdot exp(-\varphi_s/\varphi_t) + \varphi_s - \varphi_t + exp\left(-2\varphi_f/\varphi_t\right) \cdot (\varphi_t \cdot exp(-\varphi_s/\varphi_t) + \varphi_s - \varphi_t)\right)^{1/2}$ - for p-type;

$B = 2 \cdot \left(\varphi_t \cdot exp(\varphi_s/\varphi_t) - \varphi_s - \varphi_t + exp\left(2\varphi_f/\varphi_t\right) \cdot (\varphi_t \cdot exp(-\varphi_s/\varphi_t) + \varphi_s - \varphi_t)\right)^{1/2}$ – for n-type;

$F_{Si0} = (2 \cdot q \cdot N_a \cdot \varphi_t/\epsilon_{Si})^{1/2} \cdot B/\left(2\sqrt{\varphi_t}\right)$, $If \varphi_s > 0$, $F_{Si0} = -(2 \cdot q \cdot N_a \cdot \varphi_t/\epsilon_{Si})^{1/2} \cdot B/\left(2\sqrt{\varphi_t}\right)$, $If \varphi_s < 0$ - field strength near the surface;

V_{gb}=$(\epsilon_{Si}/\epsilon_{OX}) \cdot F_{Si0} \cdot T_{ox} + \varphi_s$ - gate-substrate voltage.

The results of modelling the normalised specific capacitance from the gate-substrate voltage are shown in Figure 8.

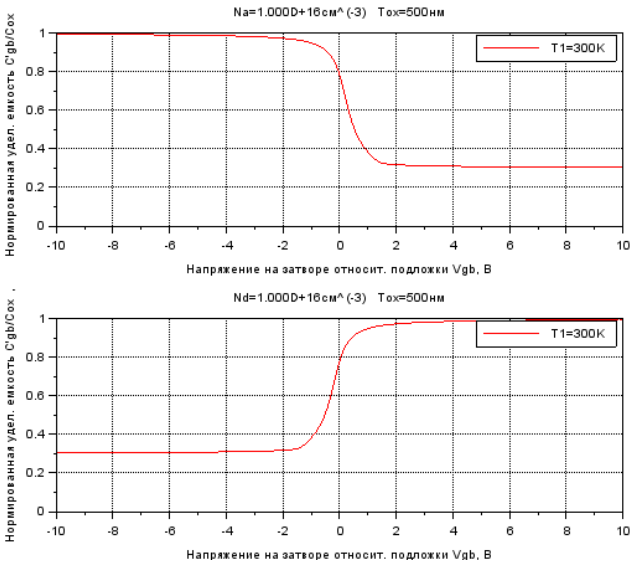

Figure 8 – Dependence of normalised specific capacitance on gate-substrate voltage for p-type (top) and n-type (bottom)

Bridge admittance meter IPPM-2. We have researched the IPPM-2 installations for automatic measurement of volt-capacitive characteristics of semiconductor structures.

Figure 9 – External appearance of the installation

The setup consists of a 1 MHz generator with an amplitude of 10 mV, a constant bias unit from -20 V to 20 V, and an RC circuit, thanks to the frequency response of which an output signal is formed, depending on the value of the measured capacitance, an amplifier and a detector.

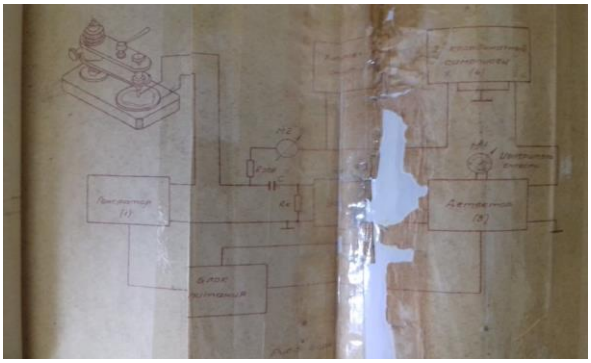

Figure 10 – Block diagram of the installation

Calibration is carried out before measurements are taken.

Figure 11 – The process of calibrating the setup using a 100 pF calibration capacitor

Modernisation of the installation to enable calibration of measurements. The industrial setup IPPM for taking volt-capacitive characteristics, which we use, is inconvenient when conducting long-term measurements due to zero drift. A trimmer resistor is provided to eliminate the zero drift, which is, unfortunately, too coarse. To consider the temperature drift, we proposed upgrading the setup to an additional electric circuit, shown in the figure, which plays the role of two channels for comparing the measured and the reference capacitance. A calibration scheme for measuring the capacitance of the IPPM-2 has been developed to modernise the measuring setup.

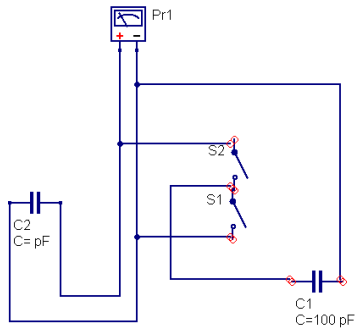

Figure 12 – Developed scheme for calibration of IPPM-2

C1 is a calibration capacitor, C2 is the sample capacitance to be measured, S1, S2 are switches, Pr1 is the input of the IPPM-2 measuring unit.

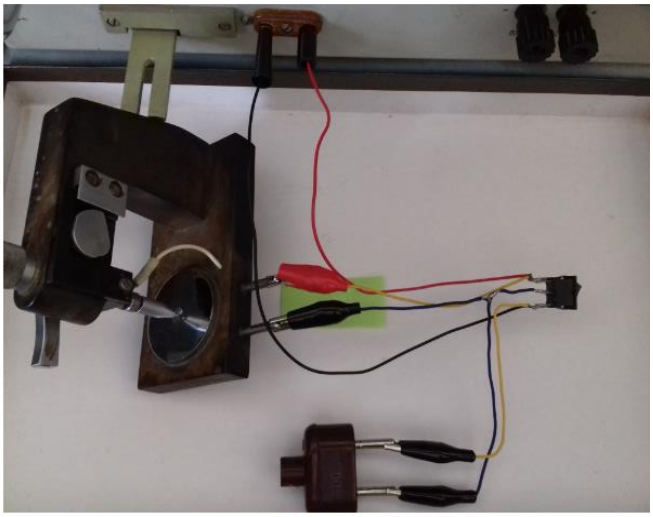

Figure 13– External view of the constructed calibration block

Calibration process. 1) After switching on the measuring setup IPPM-2, switch on S2 (off) for calibration. Rotate the screw of the variable resistor to set the value to 50 pF. 2) Switch S2 and S1 (on) for measurement

Previously manufactured MOS structures. The studied samples were p- and n-type silicon wafers with a sputtered ohmic contact, a grown oxide layer, and sputtered gates through a mask with a lattice.

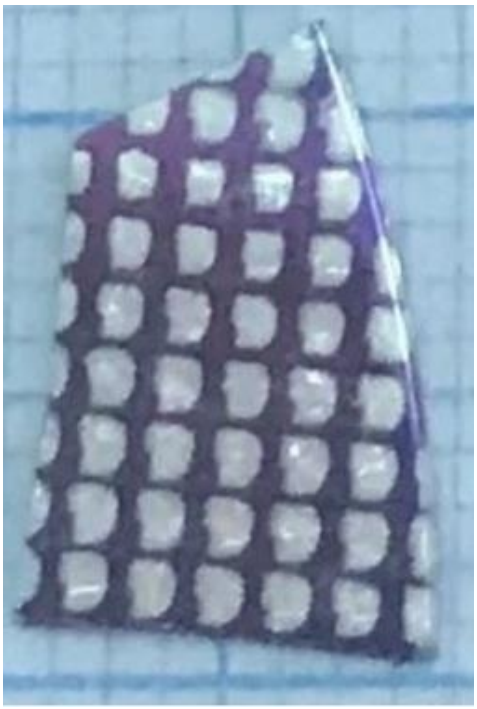

Figure 14 – The studied MOS structure (n-Si)

Using an alcohol wipe and MOP tweezers, the structure was degreased on both sides.

Figure 15 – The process of preliminary degreasing of the MOS structure with a tissue swab

A drop of water was transferred to the working table of the probe setup using tweezers to ensure electrical contact.

Figure 16 – Transferring a drop of water to ensure electrical contact

A MOP structure was placed at the location of the spreading droplet.

Figure 17 – MOS structure on the work table

Technological stage of scribing and soldering microwire to the MOS structure. To conduct further experiments at temperatures below 0ºC, it was decided to encapsulate the MOS structure to prevent condensation from getting onto the electrical contacts. The plate with many MOS structures applied to it was scribed to reduce the area occupied and save samples. Microwire contacts were glued to the MOS structure using conductive glue to eliminate mechanical contacts.

For encapsulation, the original structure was scribed.

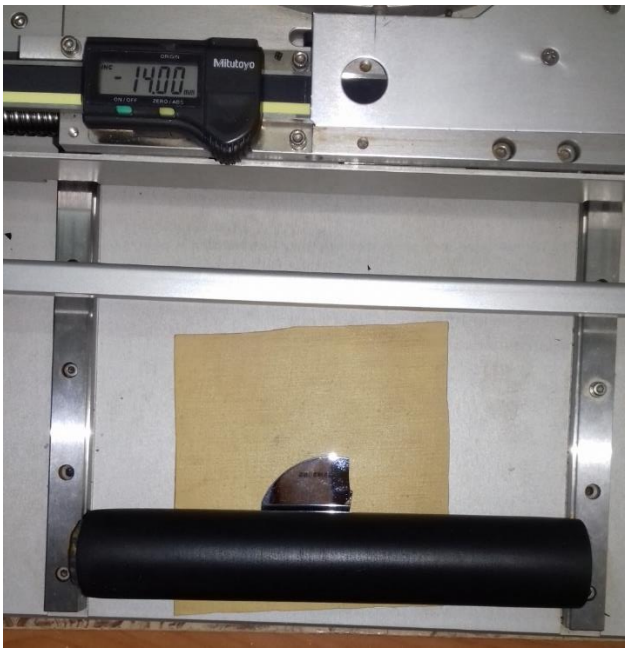

Figure 18 – Scribing process on the installation

Soldering microcontacts to the MOS structure. To form contacts from the MOS structure to the

body, it was decided to solder a copper microwire (which is part of the multi-core microwire of the cell phone headset)

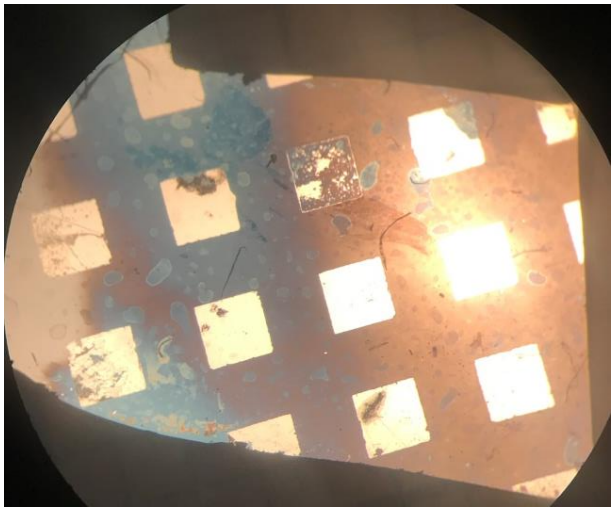

Figure 19 – Close-up view of the planar side of the MOS structure before soldering the microwave to one of the gates

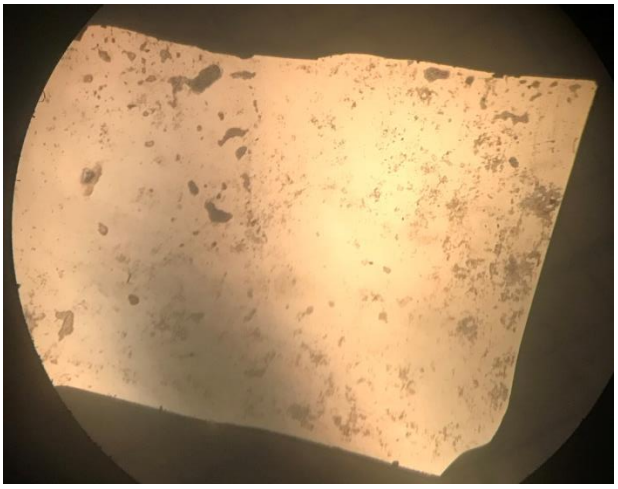

Figure 20 – Enlarged image of the structure's reverse (non-planar) side before soldering the microwave

For better adhesion of the solder, preliminary degreasing was carried out.

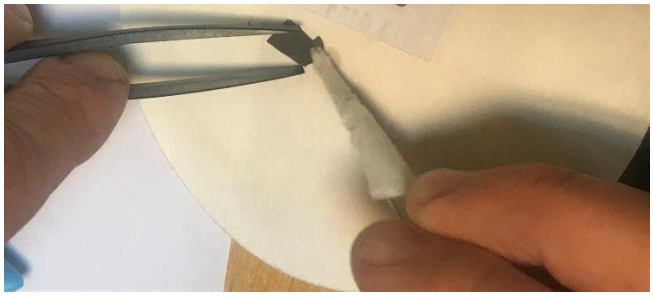

Figure 21 – Degreasing process before soldering microcontacts

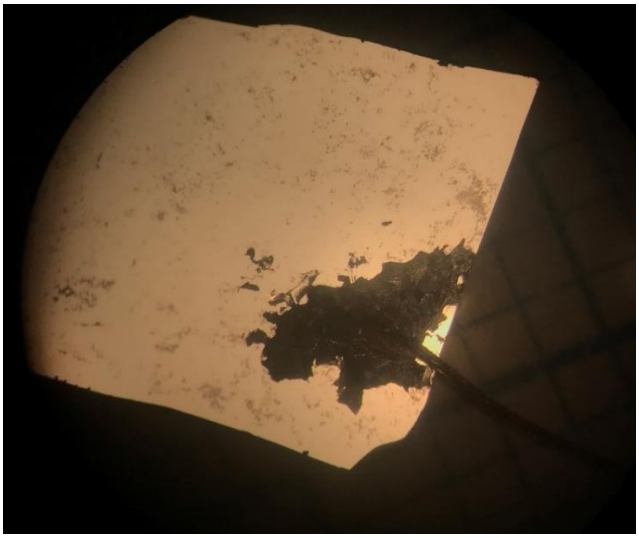

Figure 22 – Non-planar side with indium-soldered microwire

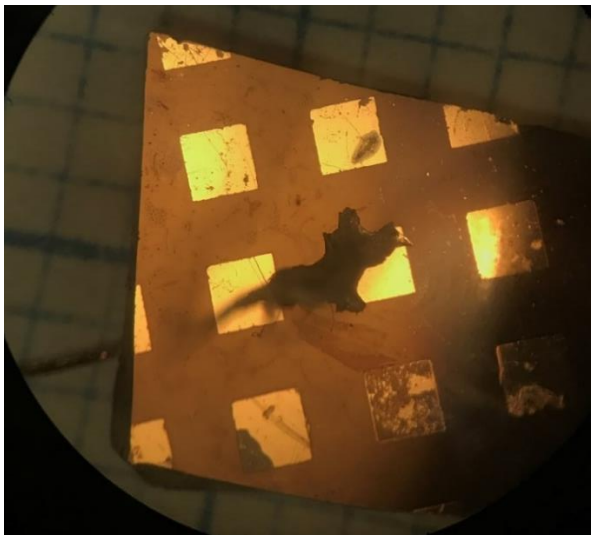

Figure 23 – Planar side with indium-soldered microwire

RESULTS AND DISCUSSION

Results measurements of the volt-capacitive characteristic of the structure:

Table 1 – Dependence of the MOS structure's capacitance on the voltage's magnitude and polarity

U, B	C, pF
-14	160
-13	160
-12	160
-11	160
-10	160
-9	160
-8	158

U, B	C, pF
-7	156
-6	154
-5	154
-4	150
-3	142
-2	140
-1	140
0	140
1	126
2	98
3	84
4	74
5	68
6	64
7	60
8	56
9	54
10	52
11	50
12	48
13	46
14	44
15	42
16	42
17	40
18	40
19	40

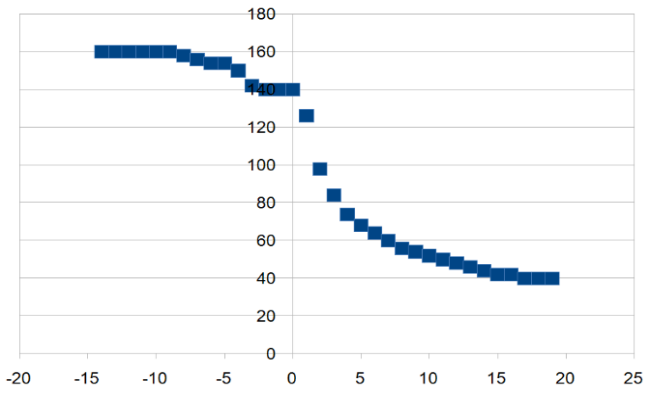

Figure 24 – CV characteristics of the MOS structure, where the horizontal axis is the gate-substrate voltage (B), and the vertical axis is the gate-substrate capacitance (pF)

1. Determine the thickness of the oxide film using the formula:

$$d = \frac{kS(\text{мм}^2)}{C_{max}(\text{пФ})} = 0.22$$

where 1 mm2 is the area of the sprayed contact; $kS = 34$ for thermal film; C_{max}= 158 pF;

2. Using the known value and the ratio taken from the volt-capacitance characteristic, we determined the concentration of the dopant in the surface layer of the semiconductor using nomogram No 1 or No 1a: $d\frac{C_{min}}{C_{max}}$

N=1.5*1014 cm^{-3}

3. For the obtained concentration and the given oxide thickness, use nomogram No 2 to determine the value of the capacitance at the point of the flat zones:

$C_{OK} = C_{max}$;$C_{FB} = 96\text{пФ}$

$$\frac{C_{FB}}{C_{OK}} = 0{,}6$$

4. Based on the experimental volt-capacitance characteristic, knowing, we determined the voltage of the flat zones of the structure C_{FB}/C_{OK} V_{FB}.

$V_{FB} = 2\text{IN}$

Scilab performed mathematical modelling of the fundamental equations describing processes in a semiconductor and for five values of the stretching factor of the capacitance-voltage characteristic graph.

Below are the results of measurements of the volt-farad characteristic for one gate and the other, superimposed on them by simulated dependencies with different stretching coefficients along the stress axis.

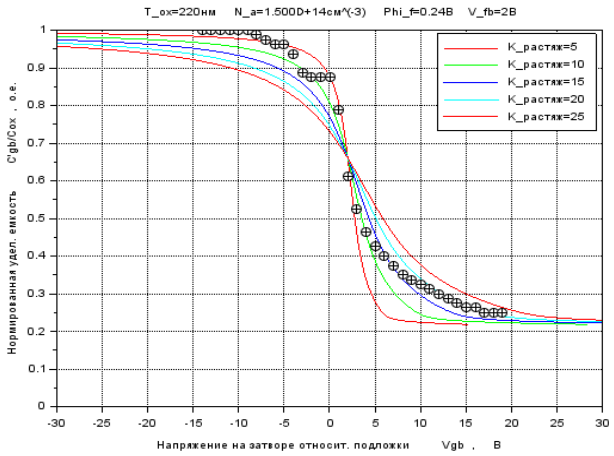

Figure 25 – Results of measurements of the volt-farad characteristic for the first gate with superimposed modelled dependencies with different stretching coefficients along the stress axis

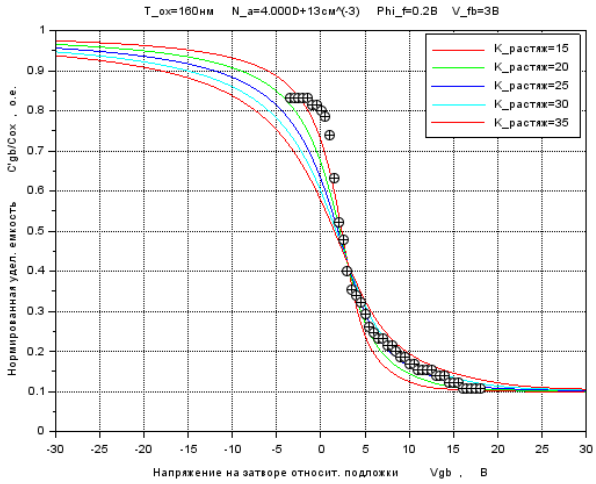

Figure 26 – Results of measurements of the volt-farad characteristic for the second gate with superimposed modelled dependencies with different stretching coefficients along the stress axis

5. Calculate the total charge density at the interface and in the dielectric using the formula:

$$Q_s\left(\frac{\text{Кл}}{\text{см}^2}\right) = \frac{\text{C}_{max}(\text{пФ})}{S(\text{мм}^2)} V_{FB}(\text{В}) 10^{-10} = 3{,}2 * 10^{-8}$$

6. Draw a tangent to the obtained volt-capacitance characteristic at a point corresponding to the flat band capacitance and determine the slope tangent. For the given concentrations and oxide thicknesses, use nomogram No 3 to determine the slope tangent of the "ideal" volt-capacitance characteristic. Determine the effective density of fast states per unit energy interval using the formula $C_{FB} tg\alpha_1 tg\alpha_2$.

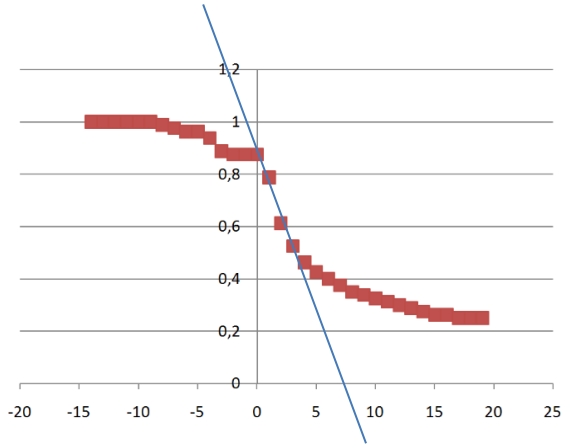

Figure 27 – Graph of determination of the tangent at the point corresponding to the capacity of flat zones CFB

$$N_{ss} = 6{,}25A\frac{C_{max}(\text{пФ})}{S(\text{мм}^2)}\left(\frac{tg\alpha_2}{tg\alpha_1} - 1\right) * 10^8 \text{см}^{-2} * \text{В}^{-1},$$

«A» is determined by Nomogram 4.

$$\text{A=4.7; S=1} tg\alpha_2 = 0.04 tg\alpha_1 = \frac{0.55}{16} = 0{,}03(\text{мм}^2)$$

$$N_{ss} = 6{,}25 * 4{,}7\frac{160}{1}\left(\frac{0{,}04}{0{,}03} - 1\right) * 10^8 \approx 1{,}5 * 10^5$$

An RF voltage with an amplitude of 1 mV was applied to one of the gates, while the DC offset value varied from -20 V to +20 V. The capacitance readings were taken on the device and entered into an Excel table, after which a graph of the volt-farad characteristic was plotted. As can be seen, the graph has a monotonous appearance with a maximum capacitance value of 50 pF and a minimum value of 34 pF.

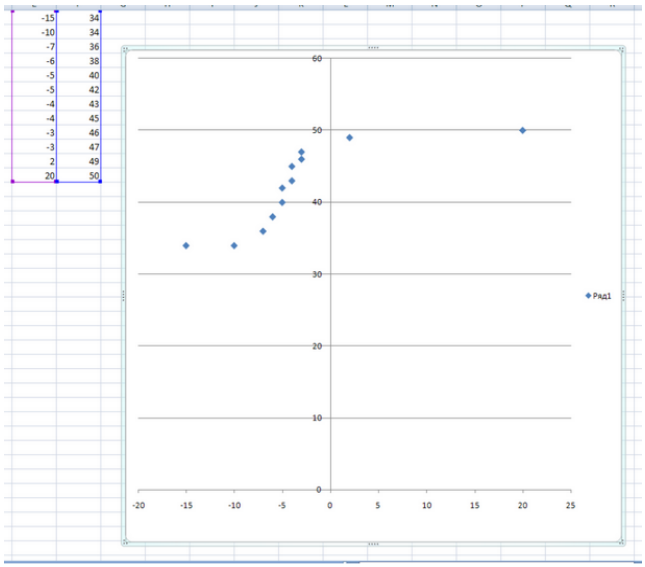

Figure 28 – Experimental high-frequency CV characteristic (horizontal axis – voltage, V, vertical axis – capacitance, pF) with a table of measured values of voltage and capacitance

CONCLUSIONS

This research investigated the parameters and characteristics of Metal-Oxide-Semiconductor (MOS) structures. The RF probing signal's capacitance-voltage (C-V) characteristics were modelled using the equation systems that describe

the processes at the metal-oxide-semiconductor interface. The study modelled the dependence of volume charge density and specific capacitance on surface potential and gate-substrate voltage for p-type and n-type structures.

The calibration technology of the measurement setup was described, and improvements to the calibration process were proposed. The sample preparation technology for measurement was detailed, and the gate area was measured to be 1 mm^2. The technological stages of scribing and soldering microwires to the MOS structure were completed.

The C-V characteristics of p-type and n-type MOS structure samples were obtained. The dopant concentration and flat-band voltage were measured. The experimental C-V characteristic was compared with the theoretical one, demonstrating that a non-zero flat-band voltage results in both a shift and an extension of the C-V characteristic along the voltage axis. The total charge at the interface and within the dielectric was also measured.

Abbreviations

q = Kl - electron charge (Electron Charge)$1{,}6.10^{-19}$

ε_0=Kl - electric constant (Permittivity of Free Space)$8{,}85.10^{-14}$

ε_{si}=11.7 - Permittivity of Siliconε_0

ε_{ox}=3.97 - Permittivity of Silicon Oxideε_0

n_i=- intrinsic carrier concentration in silicon (Intrinsic Carrier Concentration)$1{,}4.10^{10}$см$^{-3}$

N_a– Acceptor Impurity Concentration

n_0-equilibrium electron concentration

p_0- Equilibrium Hole Concentration

ϕ_f– potential difference between Fermi and the Fermi level in an intrinsic semiconductor

ϕ_t= -temperature potential (Thermal Voltage)$\frac{kT}{q}$

k=- Boltzmann's constant$1{,}38.10^{-23}$ Дж/К

T – thermodynamic temperature

ϕ_s- surface potential

$\phi(x)$- potential measured from the Fermi level (Potential)

REFERENCES

1. Grundmann, M. (2016). The Physics of Semiconductors. In *Graduate Texts in Physics*. doi: 10.1007/978-3-319-23880-7
2. Hook, J., & Hall, H. (2013). *Solid State Physics* (2nd ed.). Wiley.
3. Sze, S. M., & Ng, K. K. (2006). *Physics of Semiconductor Devices*. doi: 10.1002/0470068329
4. Sankin, V. I., Shkrebiĭ, P. P., & Lebedev, A. A. (2006). The Wannier-Stark effects in the 6H-SiC planar junction field-effect transistors with a p-n junction as the gate. *Semiconductors, 40*(10), 1237–1241. doi: 10.1134/s1063782606100204
5. Li, S. S. (Ed.). (2006). *Semiconductor Physical Electronics*. Springer New York. doi: 10.1007/0-387-37766-2
6. Attia, J. (1999). *Electronics and circuit analysis using Matlab*. Retrieved from https://www.ee.hacettepe.edu.tr/~solen/Matlab/MatLab/Matlab%20-%20Electronics%20and%20Circuit%20Analysis%20using%20Matlab.pdf
7. Stepanenko, I. (1982). *Fundamentals of Microelectronics*. Retrieved from https://archive.org/details/stepanenko-fundamentals-of-microelectronics-mir-1982
8. Bhattacharyya, A. B. (2009). *Compact MOSFET models for VLSI design*. John Wiley & Sons.
9. Springer Handbook of Electronic and Photonic Materials. (2017). In S. Kasap & P. Capper (Eds.), *Springer Handbooks. Springer International Publishing*. doi: 10.1007/978-3-319-48933-9

Application

Scilab program text for modelling the capacitive-voltage characteristics of a MOS structure

```
//MP_2_10_Cgb_Phis_Norm.m
//FIG_2.8.6
//MOS NORMALISED CAPACITANCE PER UNIT AREA VERSUS SURFACE POTENTIAL FOR ALL REGION
// DEPENDENCE OF THE NORMALIZED SPECIFIC CAPACITANCE OF A p-MOS CAPACITOR ON POTENTIAL

clear
clf

T=linspace(300,300,1)
q=1.6E-19;
eo=8.854E-14;
esi=11.7*eo;
eox=3.97*eo;
ni=1.45E10;
k=1.38E-23;
PIt_=k*T/q;
Na=1.0E+16
N.d.=1.0E+16
Tox=500E-8
Tox_nm=Tox*1e8

PIfa_=PIt_*log(Na/ni)
PIfd_=-PIt_*log(N.d./ni)
Cox=eox/Tox

color_(1)='r-'
color_(2)='g-'
color_(3)='b-'
color_(4)='c-'

forj=1:1
PIt=PIt_(j)
PIf=PIfa_(j)

PIs_=linspace(-3.,3.,1000)
fori=1:1000
PIs=PIs_(i)
```

```
A_HF=1-exp(-PIs/PIt)+exp(-2*PIf/PIt)*(0*exp(PIs/PIt)-1);
B_HF=2*sqrt(PIt*exp(-PIs/PIt)+PIs-PIt+exp(-2*PIf/PIt)*(0*PIt*exp(PIs/PIt)-0*PIs-PIt));
A=1-exp(-PIs/PIt)+exp(-2*PIf/PIt)*(exp(PIs/PIt)-1);
B=2*sqrt(PIt*exp(-PIs/PIt)+PIs-PIt+exp(-2*PIf/PIt)*(PIt*exp(PIs/PIt)-PIs-PIt));
ifPIs<0
Cc=-sqrt(2*q*esi*Na)*A_HF/B_HF;
Fsi0=-sqrt(2*q*Na*PIt/esi)*B/(2*sqrt(PIt))
else
Cc=sqrt(2*q*esi*Na)*A_HF/B_HF;
Fsi0=sqrt(2*q*Na*PIt/esi)*B/(2*sqrt(PIt))
end
CGB(i)=(Cox*Cc)/(Cox+Cc);
Vgb(i)=esi/eox*Fsi0*Tox+PIs
end

Ceq=CGB/Cox

subplot(2,1,1);plot(Vgb,Ceq,color_(j))
xlabel("Gate voltage relative to substrate Vgb, V");
ylabel("Normalized specific capacity C''gb/Cox, ");
legend(['T1='+string(T(1))+'K'])//;'T2='+string(T(2))+'K';'T3='+string(T(3))+'K';'T4='+string(T(4))+ 'K']);
title('Na='+string(Na)+'cm^(-3)'+'Tox='+string(Tox_nm)+'nm');
set(gca(),"data_bounds",matrix([-10,10,0,1],2,-1))
xgrid()

end

forj=1:1
PIt=PIt_(j)
PIf=PIfd_(j)


PIs_=linspace(-1.2,1.2,1000)
fori=1:1000
PIs=PIs_(i)
A_HF=-1+exp(PIs/PIt)+exp(2*PIf/PIt)*(1-0*exp(-PIs/PIt));
B_HF=2*sqrt(PIt*exp(PIs/PIt)-PIs-PIt+exp(2*PIf/PIt)*(0*PIt*exp(-PIs/PIt)+0*PIs-PIt));
A=-1+exp(PIs/PIt)+exp(2*PIf/PIt)*(1-exp(-PIs/PIt));
B=2*sqrt(PIt*exp(PIs/PIt)-PIs-PIt+exp(2*PIf/PIt)*(PIt*exp(-PIs/PIt)+PIs-PIt));
ifPIs<0
```

```
Cc=-sqrt(2*q*esi*N.d.)*A_HF/B_HF;
Fsi0=-sqrt(2*q*Na*PIt/esi)*B/(2*sqrt(PIt))
else
Cc=sqrt(2*q*esi*N.d.)*A_HF/B_HF;
Fsi0=sqrt(2*q*Na*PIt/esi)*B/(2*sqrt(PIt))
end
CGB(i)=(Cox*Cc)/(Cox+Cc);
Vgb(i)=esi/eox*Fsi0*Tox+PIs
end

Ceq=CGB/Cox

subplot(2,1,2);plot(Vgb,Ceq,color_(j))
xlabel("Gate voltage relative to substrate Vgb, V");
ylabel("Normalized specific capacity C''gb/Cox, ");
legend(['T1='+string(T(1))+'K'])//;'T2='+string(T(2))+'K';'T3='+string(T(3))+'K';'T4='+string(T(4))+ 'K']);
title('Nd='+string(N.d.)+'cm^(-3)'+'Tox='+string(Tox_nm)+'nm');
set(gca(),"data_bounds",matrix([-10,10,0,1],2,-1))
xgrid()

end
```